



# CODES+ISSS 2018



"view of the city of Turin" ([http://www.dianliwerml.com/posting\\_361909.html](http://www.dianliwerml.com/posting_361909.html))

## Call for Papers

International Conference on Hardware/Software Codesign and System Synthesis  
September 30 – October 05, 2018, Torino, Italy

The International Conference on Hardware/Software Codesign and System Synthesis is the premier event in system-level design, modeling, analysis, and implementation of modern embedded and cyber-physical systems, from system-level specification and optimization down to system synthesis of multi-processor hardware/software implementations. The conference is a forum bringing together academic research and industrial practice for all aspects related to system-level and hardware/software co-design. High-quality original papers will be accepted for oral presentation followed by interactive poster sessions.

### CODES+ISSS Program Chairs:

Aviral Shrivastava, Arizona State University, US  
Sudeep Pasricha, Colorado State University, US

### Topics of interest include:

**Track 1) System-level design** – Specification, modeling, refinement, system synthesis, partitioning, hardware-software co-design, design space exploration, hybrid system modelling and design, model-based design, and design for adaptivity and reconfigurability.

**Track 2) Domain and application-specific design** - Analysis, design, and optimization techniques for multimedia, medical, automotive, cyber-physical, and other specialized application domains.

**Track 3) Embedded software** - Language and library support, compilers, runtimes, parallelization, software verification, memory management, virtual machines, operating systems, real-time support, middleware.

**Track 4) Safety, security and reliability** – Cross-layer reliability, resilience and fault tolerance, test methodology, design for testability, hardware and software security, security for embedded and IoT devices, and cyber-physical system security.

**Track 5) Simulation, validation and verification** – Hardware/software co-simulation, verification and validation methodologies, formal verification, hard-

ware accelerated simulation, simulation and verification languages, models and benchmarks.

**Track 6) System architecture** - Heterogeneous systems, many-cores, networked and distributed systems, architecture and micro-architecture design, exploration and optimization including application-specific processors, reconfigurable architectures, storage, memory and communication systems, and networks-on-chip.

**Track 7) Power-aware systems** - Power- and energy-aware system design and methodologies ranging from low-power embedded and cyber-physical systems to energy-efficient large-scale systems such as cloud datacenters, green IT and smart grid.

**Track 8) Industrial practices and case studies** - Practical impact on current and/or future industries, application of state-of-the-art methodologies and tools in various application areas including wireless, networking, multimedia, automotive, cyber-physical, medical systems, etc.

A Special IoT (Internet of Things) Day will be organized jointly by all conferences in ESWEEK. Papers on IoT with the distinctive CODES+ISSS angle are very welcome and should be submitted to CODES+ISSS.

### Journal track:

Abstract submission: March 27, 2018

Full paper submission: April 03, 2018 (firm)

Notification of acceptance: July 01, 2018

### Work in Progress track:

Paper submission: May 30, 2018 (firm)

Notification of acceptance: July 01, 2018

**Workshop proposals:** March 27, 2018

**Tutorial proposals:** April 03, 2018

**Journal-integrated Publication Model:** ESWEEK 2018 will introduce a journal-integrated publication model where the majority of papers will be published in the IEEE Transactions on Computer Aided Design (TCAD).

### ESWeek General Chairs:

Soonhoi Ha, Seoul National University, KR  
Petru Eles, Linköping University, SE

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